WHAT IS CLAIMED IS:

1. A memory module comprising:

a plurality of memory devices;

a control circuit configured to generate a chip select signal that is provided to each of said plurality of memory devices, wherein said chip select signal is dependent upon assertions of a first bank chip select signal and a second bank chip select signal;

wherein said control circuit is further configured to generate an address signal that is provided to each of said plurality of memory devices, wherein said address signal is asserted dependent upon which of said first bank chip select signal and said second bank chip select signal are asserted.

2. The memory module as recited in claim 1, wherein each of said plurality of memory devices is coupled to a respective portion of a data path.

3. The memory module as recited in claim 1, wherein said control circuit is further configured to assert said address signal in response to said second bank chip select signal being asserted.

4. The memory module as recited in claim 1, wherein said control circuit is further configured to receive and decode a plurality of control signals and to generate said chip select signal in response to decoding a refresh command and detecting an assertion of said first bank chip select signal.

5. The memory module as recited in claim 1 further comprising a serially accessible storage unit configured to store information including memory module identification information.

6. The memory module as recited in claim 1 further comprising a serially accessible storage unit configured to store information including error detection information.

7. The memory module as recited in claim 6, wherein said serially accessible storage unit is a serial EEPROM.

8. The memory module as recited in claim 1 further comprising a clock circuit configured to provide clocking signals to each of said plurality of memory devices in response to receiving a pair of differential clock signals.

9. The memory module as recited in claim 1 further comprising an edge connector including a plurality of contacts providing connections between said memory module and a memory controller.

10. The memory module as recited in claim 9, wherein said first bank chip select signal and said second bank chip select signal are received at said edge connector.

11. The memory module as recited in claim 1, wherein said plurality of memory devices are logically arranged to form a single bank of sequentially addressable locations and wherein said plurality of memory devices are physically arranged in a single rank.

12. The memory module as recited in claim 11, wherein said address signal is provided to each of said plurality of memory devices for accessing an upper portion of said sequentially addressable locations.

13. The memory module as recited in claim 11 further comprising a buffer circuit configured to receive a set of address signals from a memory controller and to provide said set of address signals to said plurality of memory devices.

14. The memory module as recited in claim 13, wherein said set of address signals is provided to each of said plurality of memory devices for accessing a lower portion of said sequentially addressable locations.

15. A computer system comprising:

a processor;

a memory controller coupled to said processor;

a plurality of memory modules each coupled to said memory controller, wherein each of said plurality of memory modules includes:

a plurality of memory devices;

a control circuit configured to generate a chip select signal that is provided to each of said plurality of memory devices, wherein said chip select signal is dependent upon assertions of a first bank chip select signal and a second bank chip select signal;

wherein said control circuit is further configured to generate an address signal that is provided to each of said plurality of memory devices, wherein said address signal is asserted dependent upon which of said first bank chip select signal and said second bank chip select signal are asserted.

16. The computer system as recited in claim 15, wherein said control circuit is further configured to assert said address signal in response to said second bank chip select signal being asserted.

17. The memory module as recited in claim 15, wherein said control circuit is further configured to receive and decode a plurality of control signals and to generate said chip select signal in response to decoding a refresh command and detecting an assertion of said first bank chip select signal.

18. A method of emulating a two rank memory module using a single rank memory module, said method comprising:

receiving a first bank chip select signal and a second bank chip select signal on said single rank memory module;

generating a chip select signal and providing said chip select to each of a plurality of memory devices mounted to said single rank memory module, wherein said chip select signal is dependent upon assertions of said first bank chip select signal and said second bank chip select signal;

generating an address signal and providing said address signal to each of said plurality of memory devices, wherein said address signal is asserted

dependent upon which of said first bank chip select signal and said second bank chip select signal are asserted.

19. The method as recited in claim 18 further comprising asserting said address signal in response to said second bank chip select signal being asserted.

20. The method as recited in claim 18 further comprising receiving and decoding a plurality of control signals and generating said chip select signal in response to decoding a refresh command and detecting an assertion of said first bank chip select signal.

21. A memory module comprising:

means for receiving a first bank chip select signal and a second bank chip select signal;

means for generating a chip select signal and providing said chip select to each of a plurality of memory devices mounted to said single rank memory module, wherein said chip select signal is dependent upon assertions of said first bank chip select signal and said second bank chip select signal;

means for generating an address signal and providing said address signal to each of said plurality of memory devices, wherein said address signal is asserted dependent upon which of said first bank chip select signal and said second bank chip select signal are asserted.

22. The memory module as recited in claim 21, further comprising means for asserting said address signal in response to said second bank chip select signal being asserted.

23. The memory module as recited in claim 21 further comprising means for receiving and decoding a plurality of control signals and means for generating said chip select signal in response to decoding a refresh command and detecting an assertion of said first bank chip select signal.